TED (15) – 3133

(REVISION — 2015)

Reg. No. 17132015

Signature

DIPLOMA EXAMINATION IN ENGINEERING/TECHNOLOGY/ MANAGEMENT/COMMERCIAL PRACTICE — OCTOBER, 2018

DIGITAL COMPUTER PRINCIPLES

[*Time* : 3 hours

(Maximum marks : 100)

PART — A

(Maximum marks : 10)

Marks

I Answer *all* questions in one or two sentences. Each question carries 2 marks.

1. Define base of a number system.
2. What is parity bit ?
3. Define Encoder.
4. Define latch.
5. What is PAL ? (5×2 = 10)

PART — B

(Maximum marks : 30)

II Answer any *five* of the following questions. Each question carries 6 marks.

1. Write short notes on BCD codes.
2. State and prove De-Morgan's theorem.
3. Realize EX-OR, OR gates using NAND gate.
4. Expand A' + B' to minterms and maxterms.
5. Explain the working of a D-flipflop.
6. Differentiate synchronous and asynchronous sequential circuits.
7. Explain how memory decoding is performed. (5×6 = 30)

Marks

PART — C

(Maximum marks : 60)

(Answer *one* full question from each unit. Each full question carries 15 marks.)

UNIT — I

III (a) Convert the following :

(i) $(11011.101)_2$ to Decimal

(ii) $(BFA6)_{16}$ to binary

(iii) $(756.603)_8$ to hexa decimal 9

(b) Reduce and draw the logic diagram for the Boolean expression $F = A(B+C)+B'(B+D)$ 6

OR

IV (a) Explain basic gates with truth table and logic diagram. 9

(b) Explain the procedure of obtaining an equivalent gray code for a binary code with example. 6

UNIT — II

V (a) Simplify the Boolean function $F(w, x, y, z) = \sum m(1, 3, 7, 11, 15)$ which has the don't-care conditions $d(w, x, y, z) = (0, 2, 5)$. 9

(b) Design a half adder with truth table and logic diagram. 6

OR

VI (a) Design a decimal Adder with truth table and logic diagram. 9

(b) Write short notes on SOP and POS forms. 6

UNIT — III

VII Explain about different types of shift registers. 15

OR

VIII (a) Explain the working of a JK-Flipflop with truth table and diagram. 8

(b) Design a 3 bit up counter. 7

UNIT — IV

IX (a) Explain the specifications of a DAC. 8

(b) Explain construction of memory cell with logic diagram. 7

OR

X (a) Explain the working of programmable logic array with an example. 9

(b) Explain a R-2R ladder DAC. 6